In the Claims:

Please amend claims 1-6, 11, 13-17, 20, 21 and 23. The status of the claims is as follows:

1. (Currently Amended) A method for evaluating a floorplan and for defining a global buffered routing for an integrated circuit, the method comprising the steps of:

constructing ~~a graphical representation of~~ a tile graph from the integrated circuit (IC) floorplan, including wire capacity and buffer ~~capacity~~ capacities;

constructing a gadget graph from said tile graph such that feasible buffered routings of every net are in one-to-one correspondence to simple paths between a net source and a net sink in said gadget graph;

formulating an integer linear program from said ~~graphical representation~~ gadget graph; and

finding a solution to said integer linear program.

2. (Currently Amended) The method recited in claim 1, wherein ~~said constructing said graphical representation includes~~

~~constructing a tile graph G from the integrated circuit floorplan,~~ said tile graph ~~G including~~ comprises a tile graph G = (V, E, b, w), b → N, W: E → N, where,

V, a set of tiles v that represents the IC floorplan;

E, a set of two-dimensional edges between any two of said tiles $v \in V$ that are contiguous;

$b(v)$, a set of buffer capacities, each of said buffer capacities being a number of buffer sites located in each of said tiles $v \in V$;

$w(e)$, a set of wire capacities, each of said wire capacities being a number of wire routing channels across each of said edges $e \in E$; and

a netlist set N of nets N_i such that N = $\{N_1, N_2, \ldots, N_k\}$ to be included in the floorplan, each of said nets N_i specified by sets of source tiles $S_i \in V$, said source tiles S_i being tiles v to which at least one net source s_i may be assigned and by sets of sink tiles $T_i \in V$, said sink tiles T_i being tiles v to which at least one net sink t_i may be assigned.

3. (Currently Amended) The method recited in claim 2, ~~wherein said constructing said graphical representation further includes~~further comprising:

formulating a floorplan evaluation problem from said tile graph G, said floorplan evaluation problem including

a statement of what is given, said given statement including

said tile graph G;

said netlist N;

a wireload upper-bound of $U > 0$;

a buffer congestion upper-bound of μ_0 # 1; and

a wire congestion upper-bound of ν_0 # 1; and

a statement of what is to be found, said find statement including

feasible buffered routings (P_i, B_i), among a set R_i of all feasible buffered routings (P_i, B_i), for each of said nets N_i, each of said feasible buffered routings (P_i, B_i) including

a path $P_i = (v_0, v_1, \ldots, v_{li})$ in said tile graph G and

a set of buffers $B_i \subseteq \{ v_0, \ldots, v_{li} \}$ such that

tile $v_0 \in S_i$;

tile $v_{li} \in T_i$;

buffer capacity $b(v_i)$ ∃ 1 for every tile $v_i \in B_i$;

a length along said path P_i between tile v_0 and a first

buffer in B_i has at most said wireload upper-bound U;

a length between consecutive buffers in B_i has at most said wireload upper-bound U; and

a length between a last buffer in B_i and tile v_{l_i} has at most said wireload upper-bound U; and wherein each of said feasible buffered routings (P_i, B_i)

has a relative buffer congestion of μ # μ_0, wherein said relative buffer congestion $\mu = \max_{v \in V} \frac{|\{i : v \in B_i\}|}{b(v)}$;

has a relative wire congestion of ν # ν_0, wherein said relative wire congestion $\nu = \max_{e \in E} \frac{|\{i : e \in P_i\}|}{w(e)}$; and minimizes a total wire and buffer area.

4. (Currently Amended) The method recited in claim 3, wherein said ~~constructing a~~ gadget graph comprises a gadget graph H, said gadget graph H being constructed from said tile graph G and includes

a vertex set $V(H) = \{s_i, t_i \mid 1 \# i \# k\} \cup \{v_j \mid v \in V(G), 1 \# j \# U\}$;

and

a directed arc set $E(H)$ including

directed arc set $E_{src} = \{(s_i, v^U) \mid v \in S_i, 1 \# i \# k\}$,

directed arc set $E_{sink} = \{(v_j, t_i) \mid v \in T_i, 0 \# j \# U, 1 \# i \# k\}$,

directed arc set $E_{u,v} = \{(u^{j-1}, v^j), (v^{j-1}, u^j) \mid 1 \# j \# U\}$, and

directed arc set $E_v = \{(v^j, v^U) \mid 1 \# j \# U\}$, such that

$$E(H) = E_{src} \cup E_{sink} \cup \left(\bigcup_{(u,v) \in E(G)} E_{u,v} \right) \cup \left(\bigcup_{v \in V(G)} E_v \right).$$

5. (Currently Amended) The method recited in claim 4, wherein

said formulating ~~an~~ said integer linear program ~~from said graphical representation~~ from said gadget graph includes

denoting ~~a~~ the set of all simple paths p from said at least one net source s_i to said at least one net sink t_i as set P_i; and

formulating said floorplan evaluation problem ~~from said graphical representation~~ from said gadget graph as said integer linear program $\min \sum_{p \in P} \left(\alpha \sum_{v \in V(G)} |p \cap E_v| + \beta \sum_{(u,v) \in E(G)} |p \cap E_{u,v}| \right) x_p$, said integer linear program being subject to

$$\sum_{p \in P} |p \cap E_v| x_p \leq \mu_0 b(v), \qquad v \in V(G);$$

$$\sum_{p \in P} |p \cap E_{u,v}| x_p \leq \nu_0 w(u,v), \qquad (u,v) \in E(G);$$

$$\sum_{p \in P_i} x_p = 1, \qquad i = 1, \ldots, k; \text{ and}$$

$$x_p \in \{0,1\}, \qquad p \in P.$$

6. (Currently Amended) The method recited in claim 5, wherein

said finding ~~an integer~~ said solution to said integer linear program includes

introducing an upper-bound D on said total wire and buffer area;

formulating a linear program (min λ), said linear program (min λ) being subject to

$$\sum_{p \in P} \left(\alpha \sum_{v \in V(G)} |p \cap E_v| + \beta \sum_{(u,v) \in E(G)} |p \cap E_{u,v}|\right) x_p \le \lambda D;$$

$$\sum_{p \in P} |p \cap E_v| x_p \le \lambda \mu_0 b(v), \qquad v \in V(G);$$

$$\sum_{p \in P} |p \cap E_{u,v}| x_p \le \lambda \nu_0 w(u,v), \quad (u,v) \in E(G);$$

$$\sum_{p \in P_i} x_p = 1, \qquad i = 1, \ldots, k; \text{ and}$$

$$x_p \ge 0, \qquad p \in P; \text{ and}$$

finding a minimum upper-bound D for which an optimum objective value for said linear program (min λ) λ* # 1.

7. (Original) The method recited in claim 6, wherein

said finding a minimum upper-bound D for which an optimum objective value for said linear program (min λ) λ* ≤ 1 is performed by use of an algorithm, said algorithm simultaneously approximating said linear program (min λ) and a dual linear program

$\max \sum_{i=1}^{k} l_i$, said dual linear program being subject to

$$\sum_{v \in V(G)} \mu_0 b(v) y_v + \sum_{(u,v) \in E(G)} \nu_0 w(u,v) z_{u,v} + Du = 1;$$

$$\sum_{v \in V(G)} |p \cap E_v| (y_v + \alpha u) + + \sum_{(u,v) \in E(G)} |p \cap E_{u,v}| (z_{u,v} + \beta u) \ge l_i, \qquad p \in P_i;$$

$y_v \exists 0$, $v \in V(G)$; and

$z_e \exists 0$, $e \in E(G)$.

8. (Original) The method recited in claim 7, wherein

said algorithm finds a $(1 + \varepsilon_0)$-approximation with $O\left(\frac{1}{\varepsilon_0^2 \lambda^*} k \log n\right)$ shortest path calculations, using $\varepsilon = \min\left\{\frac{1}{\gamma}, \frac{1}{\gamma}\left(\sqrt{1+\varepsilon_0} - 1\right), \frac{1}{4}\left(1 - \left(\frac{1}{1+e_0}\right)^{\frac{1}{6}}\right)\right\}$ and

$$\partial = \left(\frac{1-\varepsilon'}{n+m}\right)^{\frac{1}{\varepsilon}},$$

wherein

n is the number of vertices of tile graph G,

m is the number of said edges of tile graph G, and

$\varepsilon' := \varepsilon(1 + \varepsilon)(1 + \varepsilon\gamma)$.

9. (Original) The method recited in claim 1, further comprising:

evaluating routing and buffer resources using said solution.

10. (Original) The method recited in claim 9, wherein

said evaluating includes computing a tradeoff curve for a total routing area, a wire congestion, and a buffer congestion.

11. (Currently Amended) The method recited in claim 1, further comprising:

defining ~~a~~ at least one feasible buffered routing using said solution.

12. (Original) The method recited in claim 11, wherein

said defining said at least one feasible buffered routing includes randomly choosing a path from among a plurality of paths yielded by said solution.

13. (Currently Amended) The method recited in claim 1, wherein said ~~graphical representation~~ gadget graph includes a representation of a flexibility for assignment of pins in the floorplan.

14. (Currently Amended) The method of claim 1, wherein said ~~graphical representation~~ gadget graph includes a representation of polarity constraints associated with inverting buffers.

15. (Currently Amended) The method recited in claim 1, wherein said ~~graphical representation~~ gadget graph includes a representation of a plurality of buffer sizes.

16. (Currently Amended) The method recited in claim 1, wherein said ~~graphical representation~~ gadget graph includes a representation of a plurality of wire sizes.

17. (Currently Amended) The method recited in claim 1, wherein said ~~graphical representation~~ gadget graph includes a representation of delay constraints.

18. (Original) The method recited in claim 1, wherein said finding a solution to said integer linear program includes finding a solution for at least one net with a single source and a single sink.

19. (Original) The method recited in claim 1, wherein said finding a solution to said integer linear program includes finding a solution for at least one net with a single source and a plurality of sinks.

20. (Currently Amended) The method recited in claim 1, wherein ~~constructing said graphical representation includes constructing a~~ said tile graph ~~having~~ includes tiles of a plurality of sizes.

21. (Currently Amended) The method recited in claim 1, wherein said ~~graphical representation~~ tile graph includes a representation on constraints on a numbers of buffers in specified sets of tiles.

22. (Original) A computer-readable medium having computer-readable instructions for performing the method recited in claim 1.

23. (Currently Amended) A method for evaluating a floorplan and for defining a global buffered routing for an integrated circuit, the method comprising the steps of:

~~constructing a graphical representation of the integrated circuit floorplan, said constructing including~~

constructing a tile graph from the integrated circuit floorplan,

formulating a floorplan evaluation problem from said tile graph, and

constructing a gadget graph from said tile graph such that feasible buffered routings of every net are in one-to-one correspondence to paths between net source and a net sink in said gadget graph;

formulating said floorplan evaluation problem as an integer linear program from said ~~graphical representation~~ gadget graph; and

finding a solution to said integer linear program, ~~said finding~~ including,

finding a solution to a fractional relaxation of said integer linear program, and

rounding said solution to said fractional relaxation to an integer solution using randomized rounding.

24. (Original) A computer-readable medium having computer-readable instructions for performing the method recited in claim 23.